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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/531,399
Filing Date: April 14, 2005
Appellant(s): KLOSTERS ET AL.

Michael Ure, Reg. No. 33,089
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/12/2008 appealing from the Office action mailed 10/10/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Hongbin Hao et al. (U.S. 6,163,586) and Wishneusky et al. (U.S. 4,975,828) are relied upon as evidence.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Maintained Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, and 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hongbin Hao et al. (U.S. 6,163,586, hereinafter Hao).

3. As per claim 1:

Hao disclosed a data processing apparatus, the apparatus comprising:

An input port for receiving a communication signal that contains temporally successive bits (Hao: Figures 3-4 element 14, column 3 lines 38-41 and column 6 lines 51-63)(Temporally successive bits is interpreted as successive bits received over time. Input element 14 receives serial bits as shown in figure 3.);

An output port for outputting a data word formed from respective ones of the temporally successive bits (Hao: Figures 3-4 element 16, column 3 lines 38-41 and column 7 lines 11-14)(Output element 16 receives the data word and echo's it through.);

A programmable processor circuit coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving or said outputting (Hao: Figures 4-5 element 20)(Element 20 is coupled to element 14 and is programmable since it's originally programmed prior to fabrication. An instruction in

its broadest sense is a command and/or explanation of how to perform a given task. In this definition, instructions are present within the state diagram of figure 5 to perform comparisons to detect certain given characters at elements 58, 68, 70, and 80. These comparisons make up the series of programmed instructions.), each at a time of reception of a respective ones of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions (Hao: Figures 3 and 5 elements 56, 64, 70, and 80, column 7 lines 51-60)(The processor is suspended between start bits as shown in figure 3 and elements 56 and 64. The processor is also temporarily suspended after instructions 70 and 80.);

A synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective ones of the temporally successive bits (Hao: Figures 4-5 elements 32, 56, and 64, column 7 lines 11-27)(Element 32 performs the determining steps of elements 56 and 64, which determines if a start bit is within a legal window. If a start bit is within a legal window, this triggers the state diagram to continue to elements such as 58, 68, 70, and 80 that perform a series of instructions.), and, except for a last one of the series, prior to reception of one or more later bits that contribute to the data word (Hao: Figure 4 elements 14, 20, 22, and 32)(It's inherent that for a last bit of the series, it must be received via element 14 prior to having any actions performed on it by elements 20, 22, and 32.).

4. As per claim 2:

Hao disclosed a data processing apparatus according to claim 1, wherein the programmable processor (element 12 figure 4) is programmed to compute cumulative information [the state in the flow diagram of figure 5], corresponding to a function of a combination of the bits from which the data word is formed [the determination of the character received from the received bits (column 7 line 60 to column 8 line 17)], each series of instructions being programmed to add a contribution (the new state in the flow of figure 5) to the cumulative information (the old state in the flow of figure 5) of the respective ones of the temporally successive bits at the time of reception of which the series is executed [the changing state in the flow depending on the series of bit received previously (column 7 line 60 to column 8 line 17)].

5. As per claim 4:

Hao disclosed a data processing apparatus according to claim 1, wherein the processor circuit is constructed sequence instruction execution [the operation executed by the circuit depends on the state of the flow in figure 5]; the operation is inherently triggered by some signals (using handshake signals), execution of each of the instruction in the series being triggered by a respective request signal [each operation is triggered by receiving a new data bit through input port (column 7 line 60 to column 8 line 17)], execution of each instruction of the series, except for a last instruction in each series, generating the request signal for a next one of the instructions in the series [each operation trigger a next step or repeat the same operation (active wait) (figure 5)], the synchronization circuit being coupled to apply the request signals for the initial one

of the instructions in the series [the synchronization circuit receives the signal coming into the input port (column 6 lines 62-66) and the circuit trigger the operation in the flow].

6. As per claim 5:

Hao disclosed a data processing apparatus according to claim 1, wherein the synchronization circuit (element 32, 20 figure 4) is arranged to adapt a frequency of triggering the execution of the series of instructions under control of a timing of transitions in the communication signal [the incoming signal is analysis to determine the value of M by the baud rate determination means and the value of M is sent to the synchronization circuit (column 7 lines 13-26) through the usage of value M (BT, BT=32M column 7 lines 57-60) the synchronization circuit is adapt to the frequency to sample the data input (column 7 line 60 to column 8 line 17) thus triggering the operation in changing in flow of figure 5], since the synchronization circuit is arranged to operate as such, it is inherent that it contains an adaptable timer circuit.

7. As per claim 6:

Hao disclosed a data processing apparatus according to claim 5, wherein the synchronization circuit inherently has the adaptable timer circuit (see rejection of claim 5), and the circuit is arranged to measure a duration of a synchronization interval in the communication signal preceding bits (start bits) that contribute to the data word [measure the duration of the start bit to determine the baud rate (column 7 line 60 to column 8 line 17)], and to set the frequency that will be used to trigger execution of the series of instructions dependent on the measured duration [the synchronization circuit is

adapt to the frequency to sample the data input (column 7 line 60 to column 8 line 17) thus triggering the operation in changing in flow of figure 5].

8. As per claim 7:

Hao disclosed a data processing apparatus according to claim 6, wherein the timer circuit is arranged to detect presence or absence of a validation part (start bits) in the communication signal prior to bits that contribute to the data word (start bit is not part of the character received), the timer circuit generating execution trigger signals only upon detection of the presence of the validation part [timer circuit would not calculate value of M and BT till the detection of start bits thus would not enable the synchronization circuit to further trigger operation in the flow of figure 5 (column 7 lines 47-64)].

9. As per claim 8:

Hao disclosed a data processing apparatus according to claim 1, wherein the processor circuit (element 12 figure 4, The operand length, is not patentably distinct as it is possible that the operand length of the instruction executed by the processor in the prior art could be changed and there would be no difference in performance over the processor of the prior art. See MPEP 2144.04 section IV).

10. As per claim 9:

The additional limitation(s) of claim 9 basically recite the additional limitation(s) of claim 1. Therefore, claim 9 is rejected for the same reason(s) as claim 1.

Maintained Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hongbin Hao et al. (U.S. 6,163,586), further in view of Wishneusky et al. (U.S. 4,975,828).

13. As per claim 3:

Hao disclosed a data processing apparatus according to claim 2.

Hao failed to teach said cumulative information comprises one or more parity bits.

However, Wishneusky disclosed a data processing apparatus (figure 2) that support the calculation of parity in a cumulative bit by bit fashion (column 27 lines 21-25, column 29 lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the cumulative calculation parity instruction into the series to series of instructions to calculate parity as part of the cumulative information in the apparatus of Hao because Wishneusky teaches that inclusion of such instruction can help the apparatus performance in time critical task associated with receiving and sending of data word (Wishneusky column 6 lines 28-32). Including the cumulative calculation of parity further enhances the speed of the method of baud rate detection

and character configuration in Hao by speeding up the process of assembling the incoming predetermined characters (AT or at) (Hao column 1 lines 59-64).

(10) Response to Argument

14. Regarding claims 1-2, and 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hongbin Hao et al. (U.S. 6,163,586, hereinafter Hao):

A.) Applicant argues "At the most basic level, a principal difference between Hao and the present invention is that the processor of the present invention is programmable, whereas the apparatus of Hao is dedicated, or hardwired. The use of dedicated or hardwired bit processors is described in the BACKGROUND portion of the present specification."

The examiner partially agrees for the following reasons. The examiner agrees that the processing logic of Hao involves dedicated hardware. However, the Autobaud State Machine element 20 in figure 4 is one-time programmable to perform the task that is shown in figure 5. Thus, the Autobaud State Machine is a programmable processor circuit.

The applicant's specification on page 1 lines 20-22 talks of a programmable processor that may allow for changes to processing functions. This type of processor is a reprogrammable processor that allows for functions to be programmed more than once. However, this interpretation isn't the broadest reasonable interpretation of the claimed limitation "programmable processor," which only requires the processor to be programmed once.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., programmable processor capable of changing functions) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

B.) Applicant argues "The autobaud state machine does not execute a series of programmed instructions. Nor does the autobaud module 12 as a whole "execute a plurality of series of programmed instructions in support of said receiving or said outputting.""

The examiner disagrees for the following reasons. The broadest reasonable interpretation of instruction is a command and/or explanation of how to perform a given task. Thus, a programmed instruction is a programmed command and/or explanation of how to perform a given task. In this definition, instructions are present within the state diagram of figure 5 to perform comparisons to detect certain given characters at elements 58, 68, 70, and 80. These comparisons are programmed to be performed into the state diagram element 20 in figure 4. The series of instructions occurs when executing these comparison instructions in series. This is clearly shown in figure 5 where instructions at elements 58, 68, 70, and 80 are executed in series. Thus, Hao disclosed the limitation "a programmable processor circuit coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving or said outputting."

C.) Applicant argues "Hao failed to teach each at a time of reception of a respective one of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions. The autobaud state machine, in particular, is incapable of suspending operation. A state machine "waiting" for the start bit of a next character is certainly not the same as suspending operation. "

The examiner disagrees for the following reasons. The definition of suspending is to bar or stop temporarily. Thus, suspending operation is to bar or stop operation temporarily. There are multiple points in the state machine in figure 5 that read upon the claimed limitation.

In figure 5, an instruction occurs at element 58. A suspension of operations results each time this instruction is executed either by waiting through element 88 or waiting for the next character at element 62. A temporary suspension of execution of the instructions occurs in either case.

In figure 5, one of the temporally successive bits is received at element 66. A suspension of operations results when the comparison instruction at element 80 finishes executing. Operations are temporarily suspended either through the waiting element 88 or through turning the autobaud off at element 78.

Similar logic can be used to show that operations suspend when executing instructions at elements 68 and 70.

Finally, the specification on page 4 lines 24-31 discloses a typical series of instructions, including a wait instruction. The wait instruction causes suspension of

operations until a next bit (presumably, until the next bit arrives). Thus, the specification clearly shows that waiting for a next bit is the same as suspension of operations.

D.) Applicant argues "Hao failed to teach a synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective ones of the temporally successive bits."

This argument is not found to be persuasive for the following reason. Element 32 performs the determining steps of elements 56 and 64, which determines if a start bit is within a legal window. Detecting the start bit synchronizes the autobaud sequence to follow in figure 5. Synchronizing occurs by ensuring the autobaud sequence occurs every time a start bit is detected. If a start bit is within a legal window, this triggers the state diagram to continue to elements such as 58, 68, 70, and 80 that perform a series of instructions. Thus, Hao correctly reads upon the claimed limitation.

E.) Applicant argues "In fact, there are no instructions in Hao, programmable or otherwise. A sequence of instructions are stored in advance and a particular instruction is selected for execution at a particular time. Note, for example, the structure of the processor 100 of Fig. 6 of the present specification. A program counter 48 applies an address to an instruction memory 102, which applies a selected instruction to a logic unit 42. Such a construction is characteristic of a processor that executes instructions. There is no corresponding structure in Hao. Rather, in Hao, as in any typical state machine, there are state registers 24, the contents of which are changed to register

state changes during the course of operation of the state machine. There are no instructions stored in advance."

The examiner disagrees for the following reasons. As discussed in paragraph B, the broadest reasonable interpretation of instruction is a command and/or explanation of how to perform a given task. Thus, a programmed instruction is a programmed command and/or explanation of how to perform a given task. In this definition, instructions are present within the state diagram of figure 5 to perform comparisons to detect certain given characters at elements 58, 68, 70, and 80. Thus, Hao disclosed programmable instructions.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., sequence of instructions stored in advance and structure from figure 6) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jacob A. Petranek/

/JAP/

June 10, 2008

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